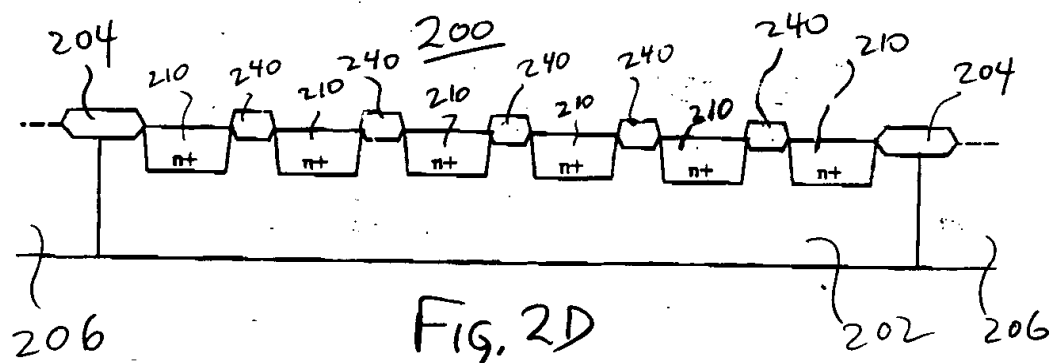
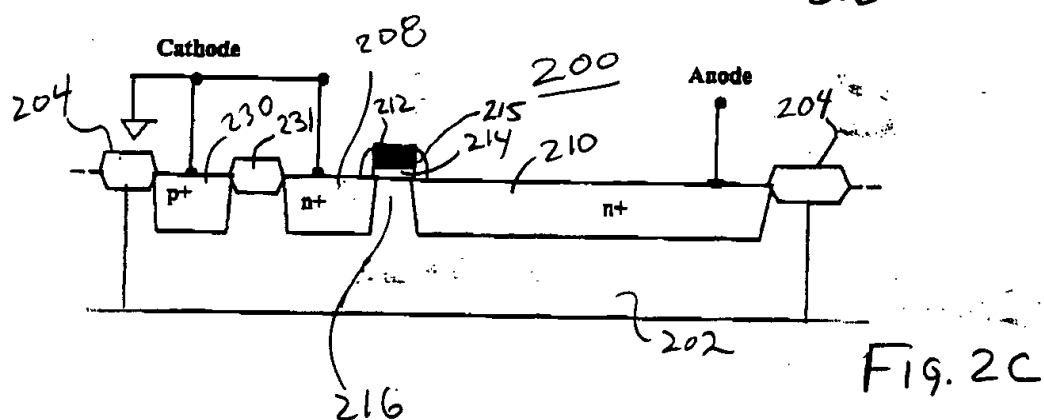
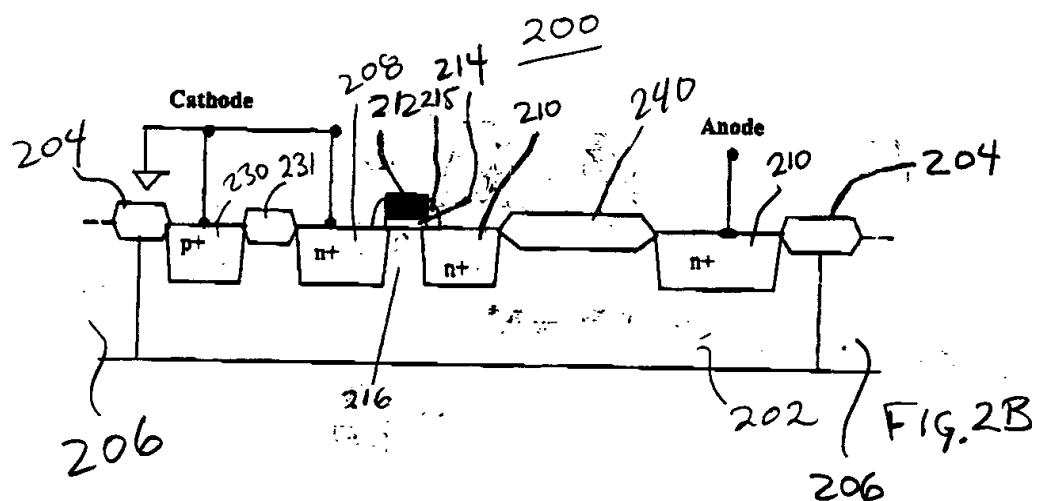


The diagram illustrates a 1T1R1C1 array cell (400). It features a central access transistor (40a-40g) connected to word lines (42a-42h) and bit lines (44a-44h). The access transistor is controlled by a gate voltage (G) and has a width (W) and length (L). The bit lines are connected to a VSS BUS. The word lines are connected to a VDD/I=0 supply. The diagram also shows a hatched region (41) and a label (42) for the word lines. A handwritten note 'PRIORITY' is present at the bottom.

PRIOR ART

Fig. 1





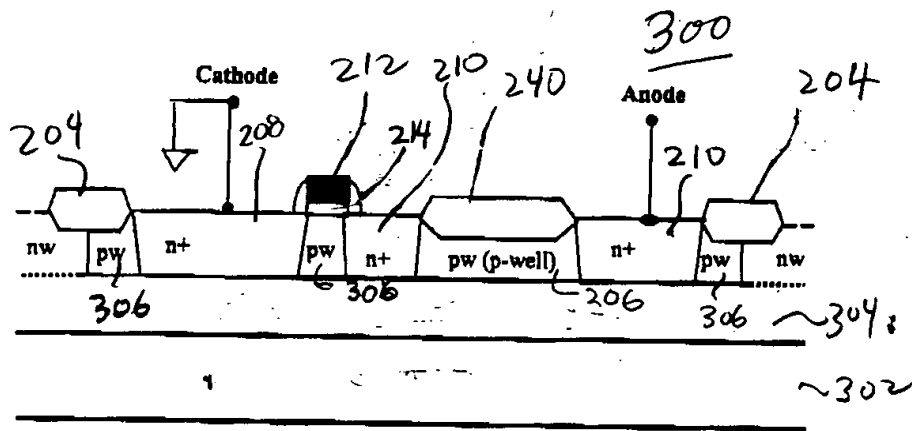


Fig. 3A

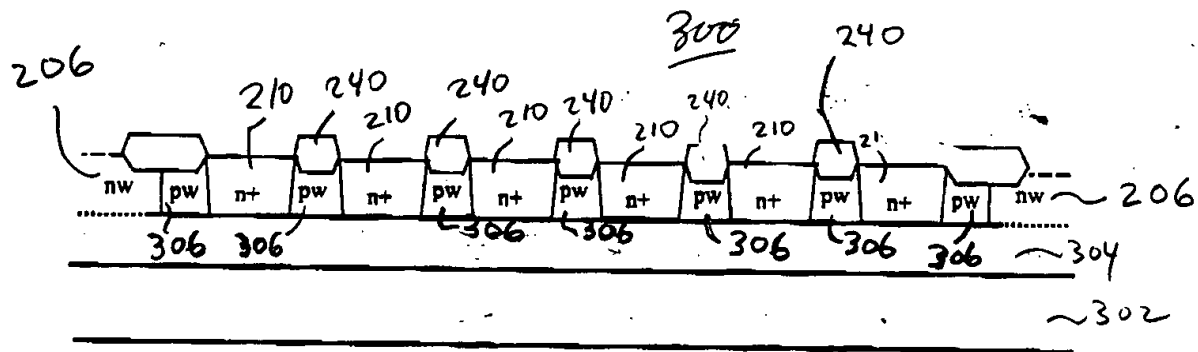


Fig. 3B

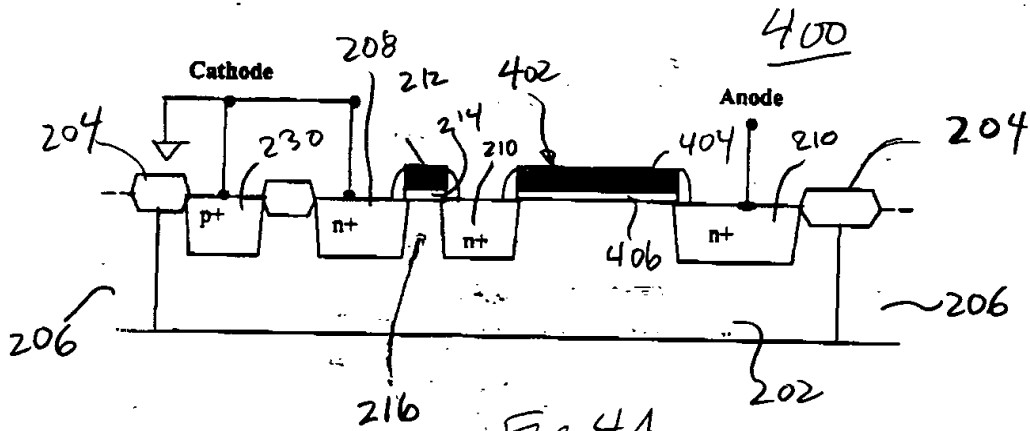


Fig. 4A

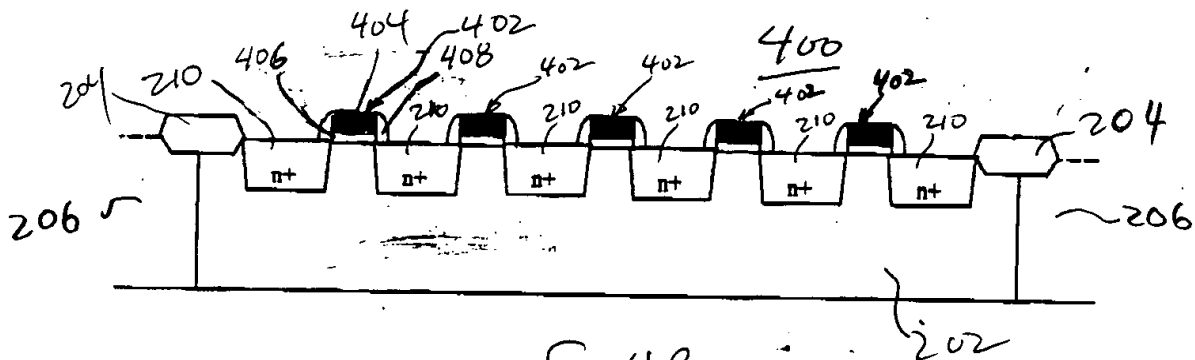


Fig. 4B

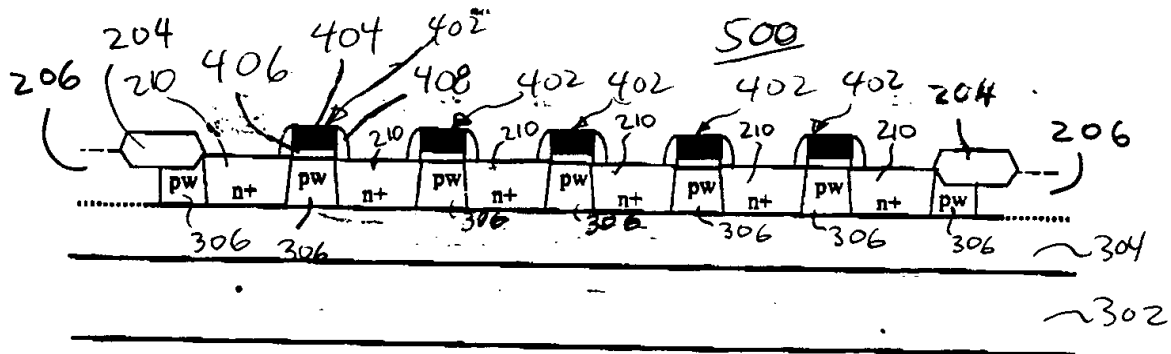


Fig. 5

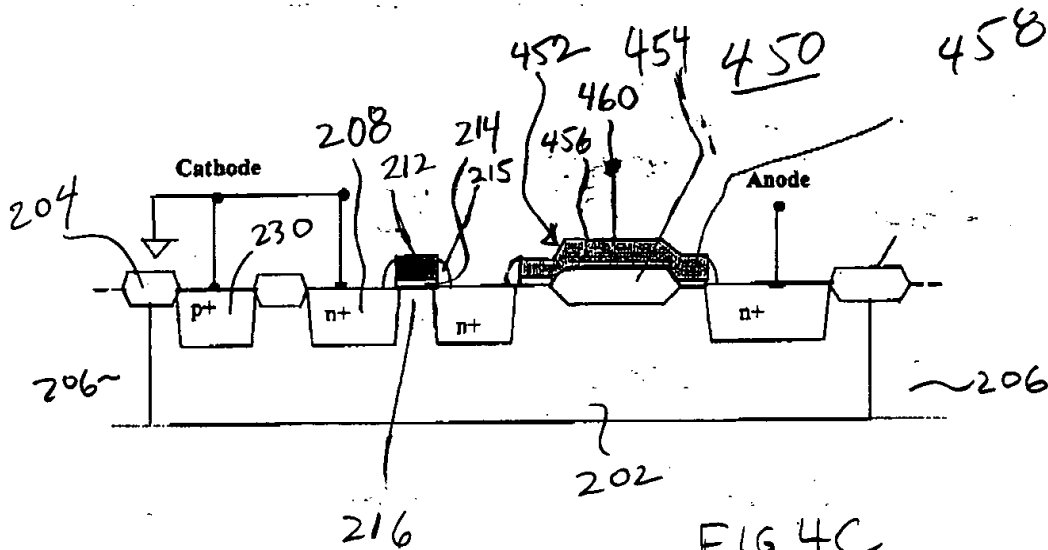


FIG. 4C

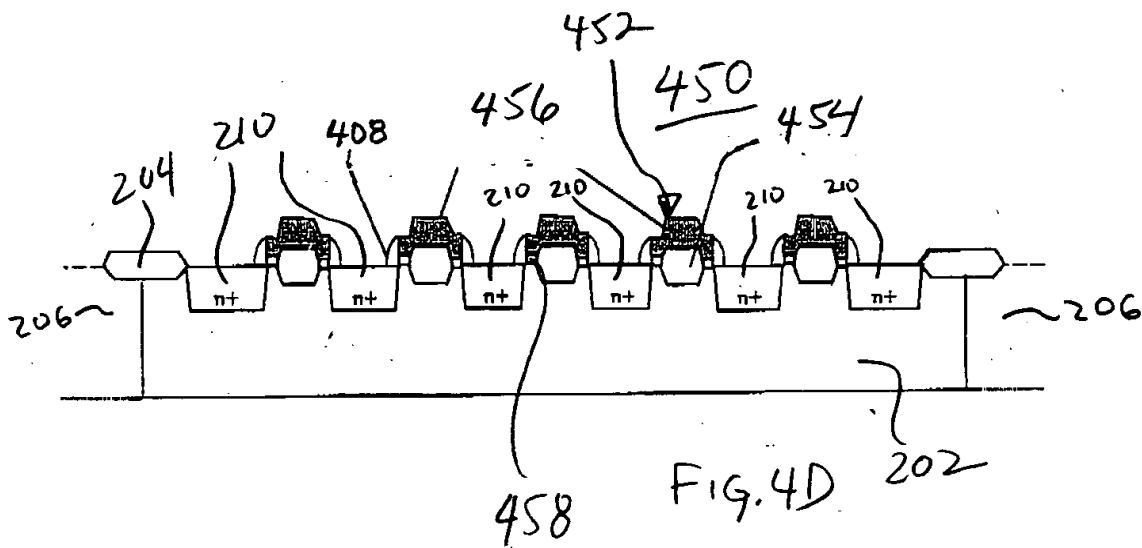


FIG. 4D

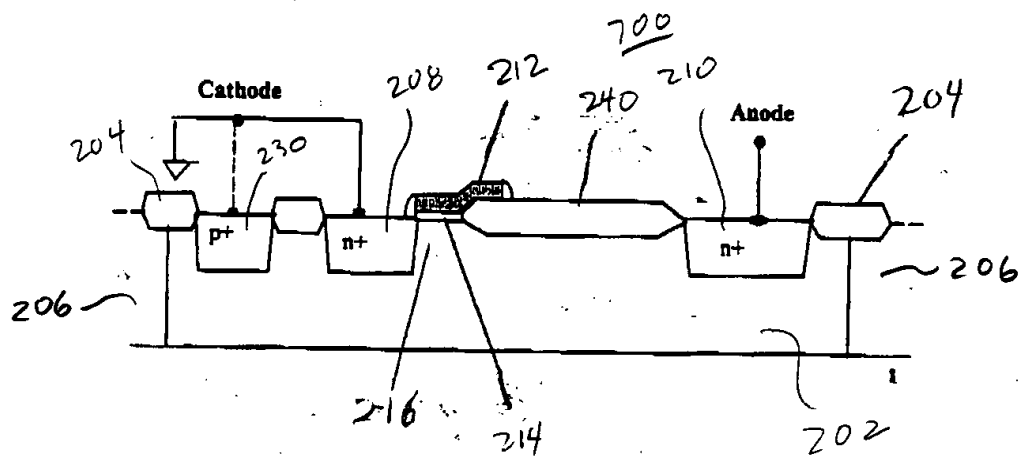
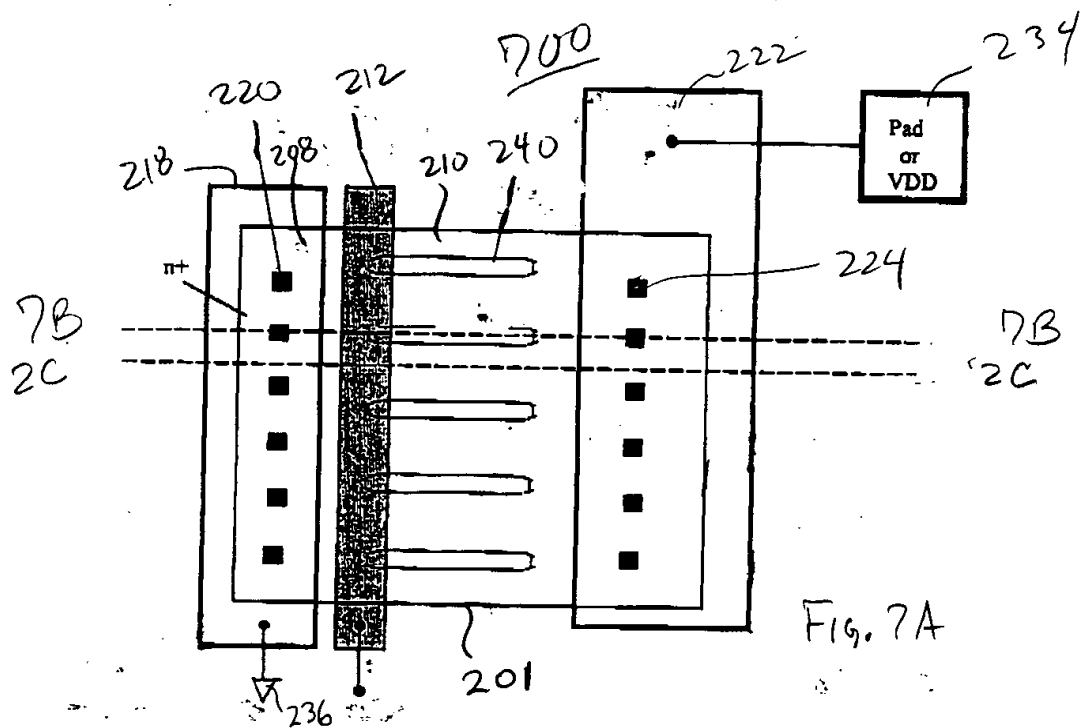


Fig. 7B

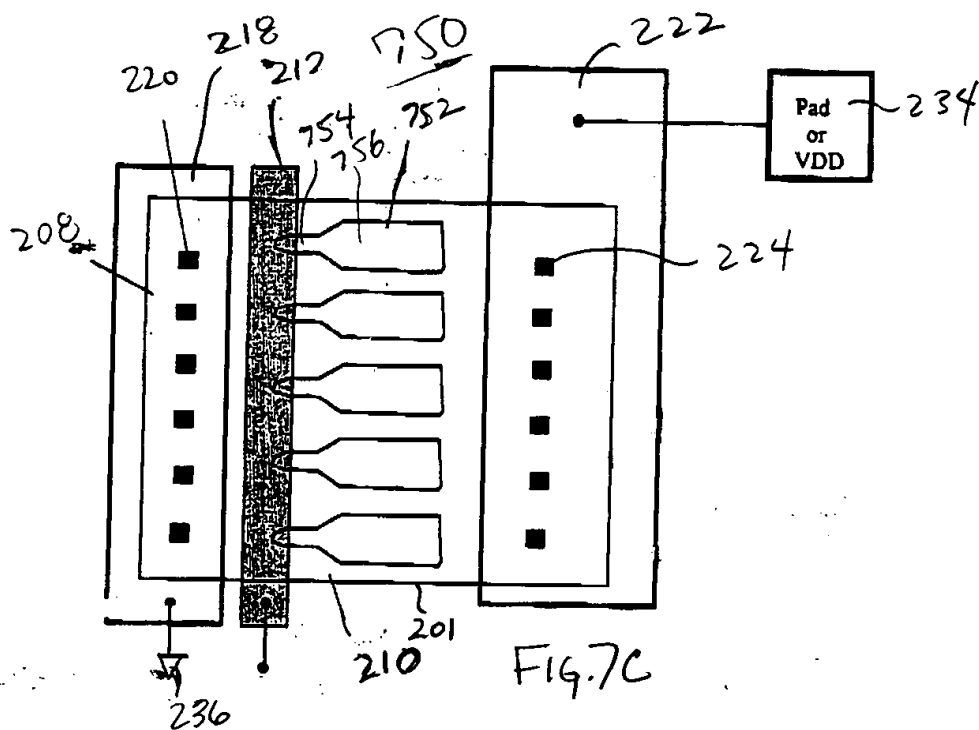


Fig. 7C

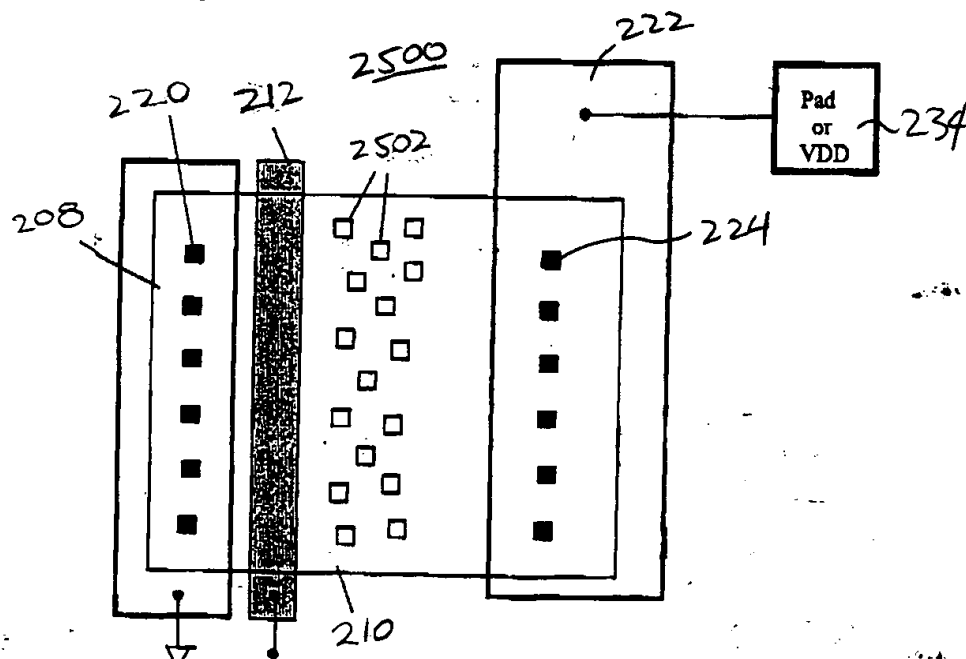
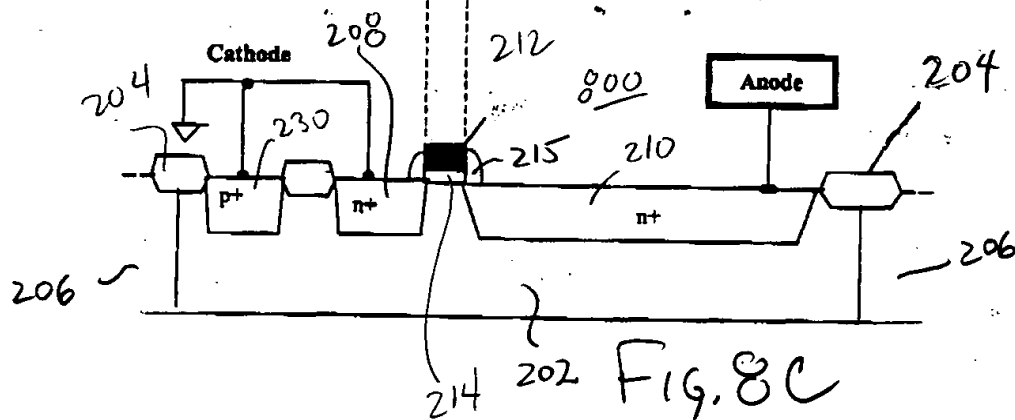
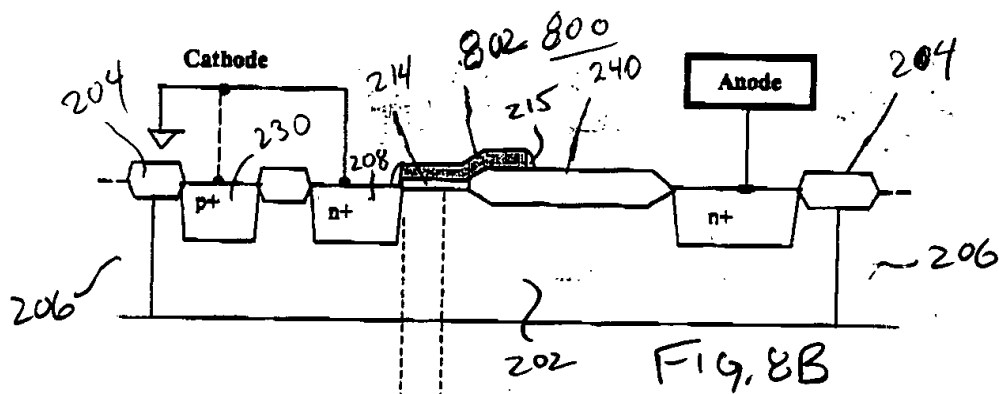
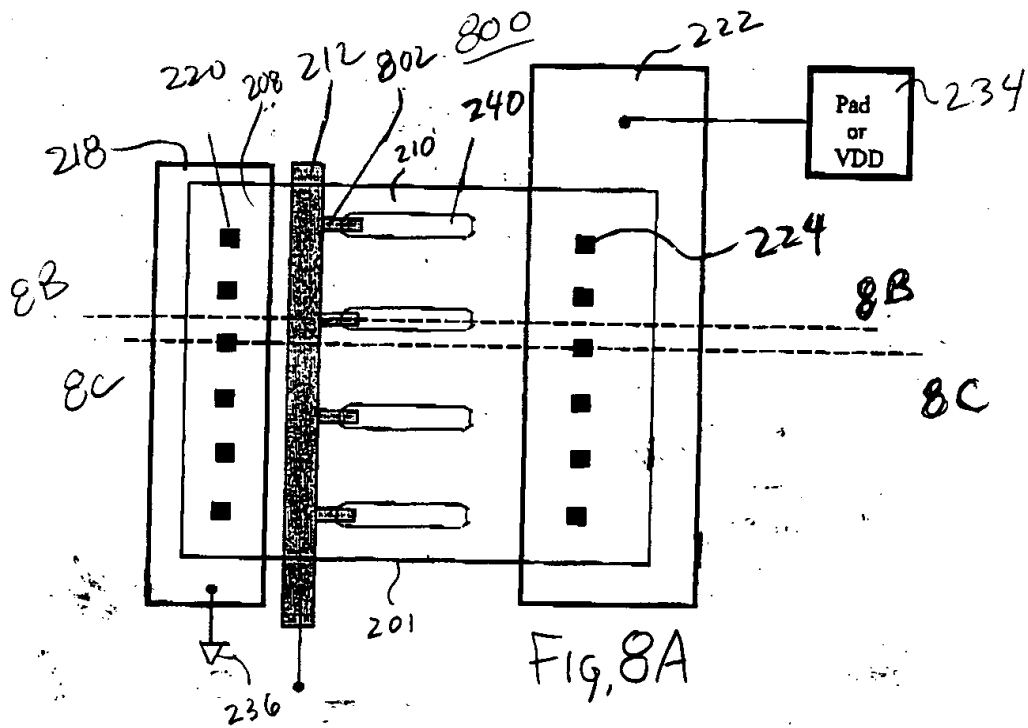


Fig. 25





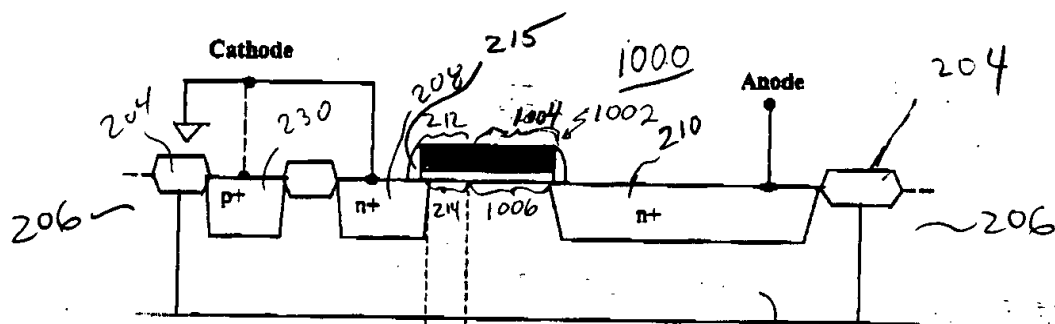
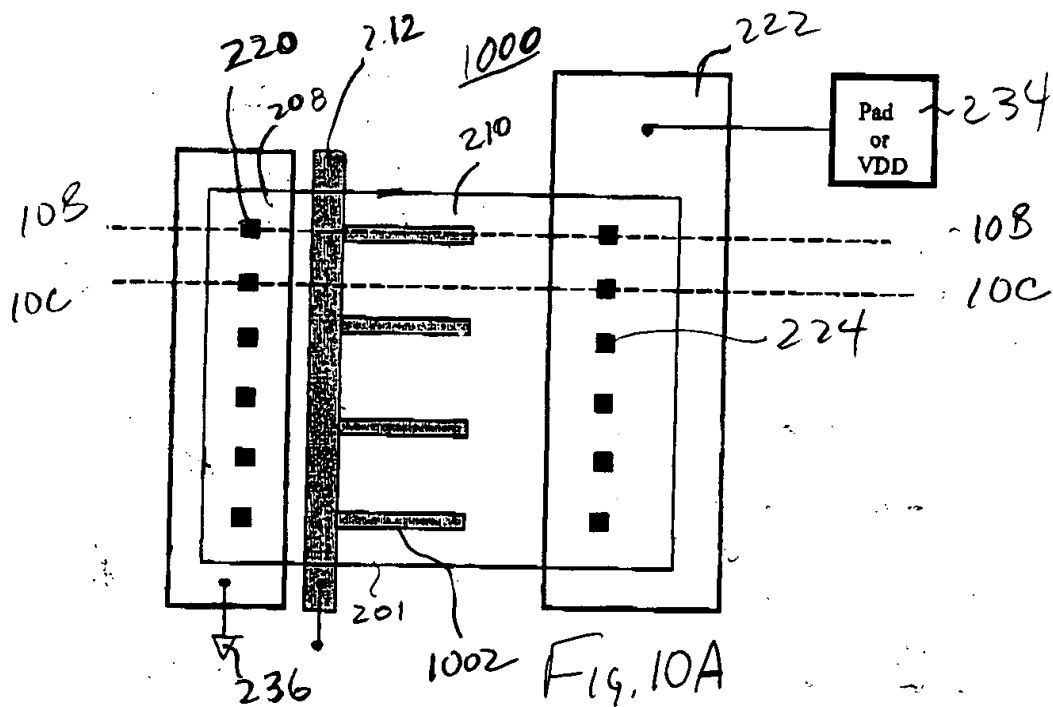


Fig. 10B 202

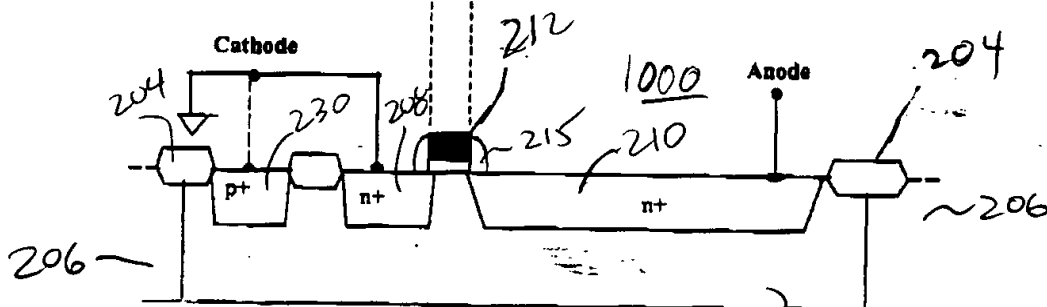
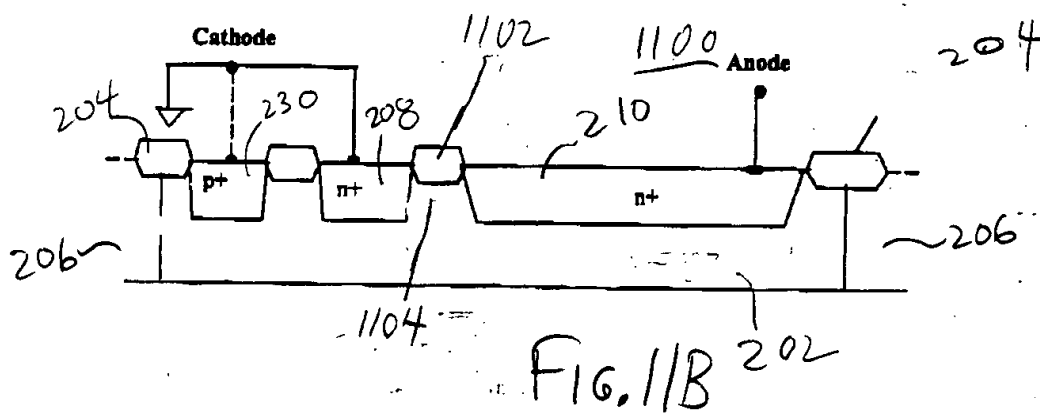
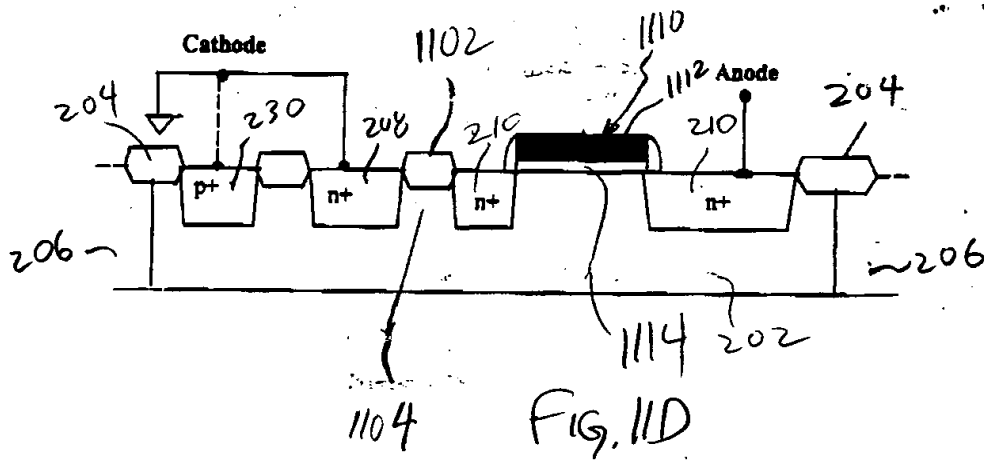
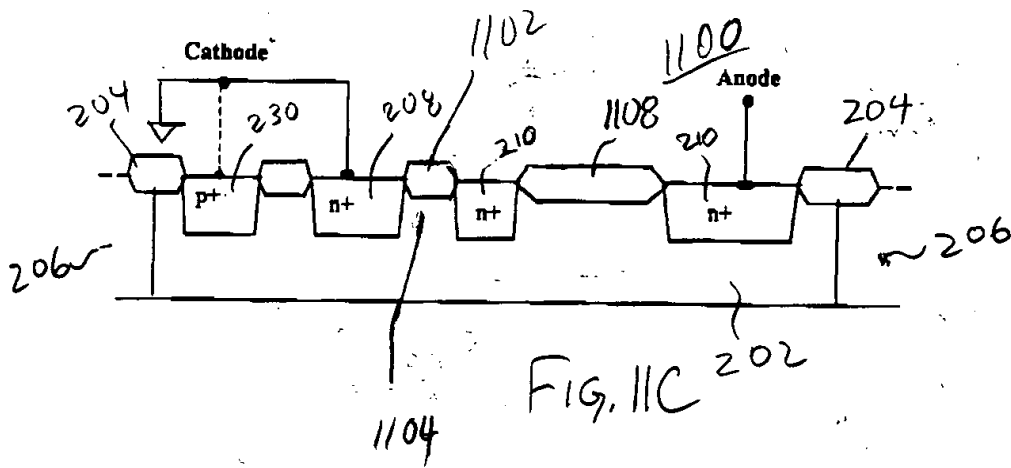


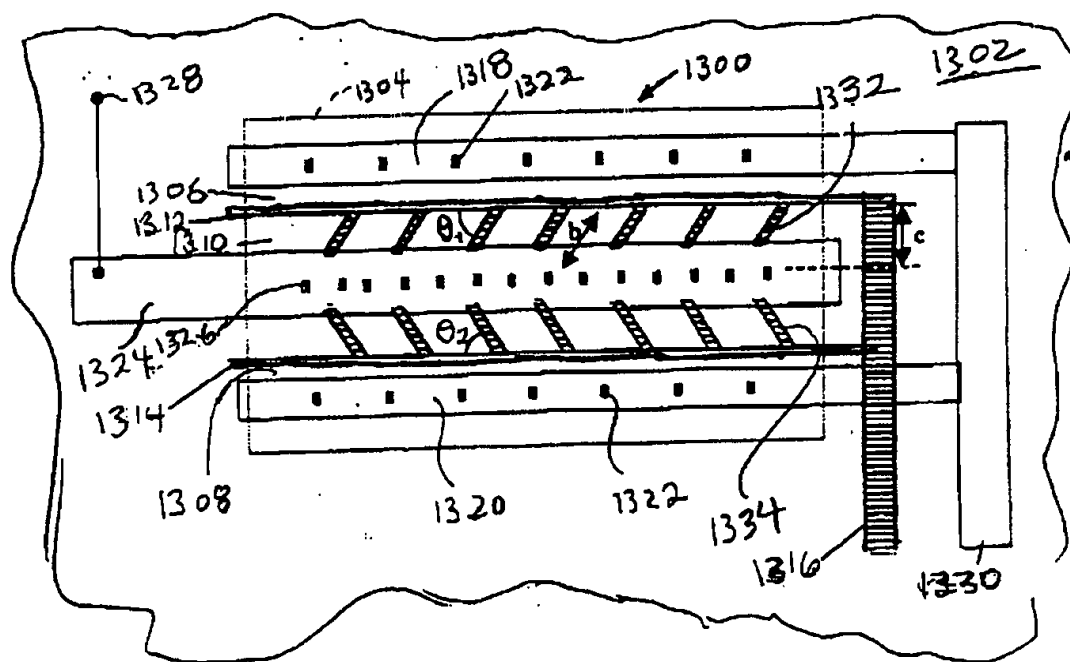
Fig 10c 202





200315767263





S.L. 12-14, 20

CHL  
Dec. 14, 2001

WFC.

Dec. 14, 2001

WYU.

Dec. 16, 200

Fig. 13

[illegible]

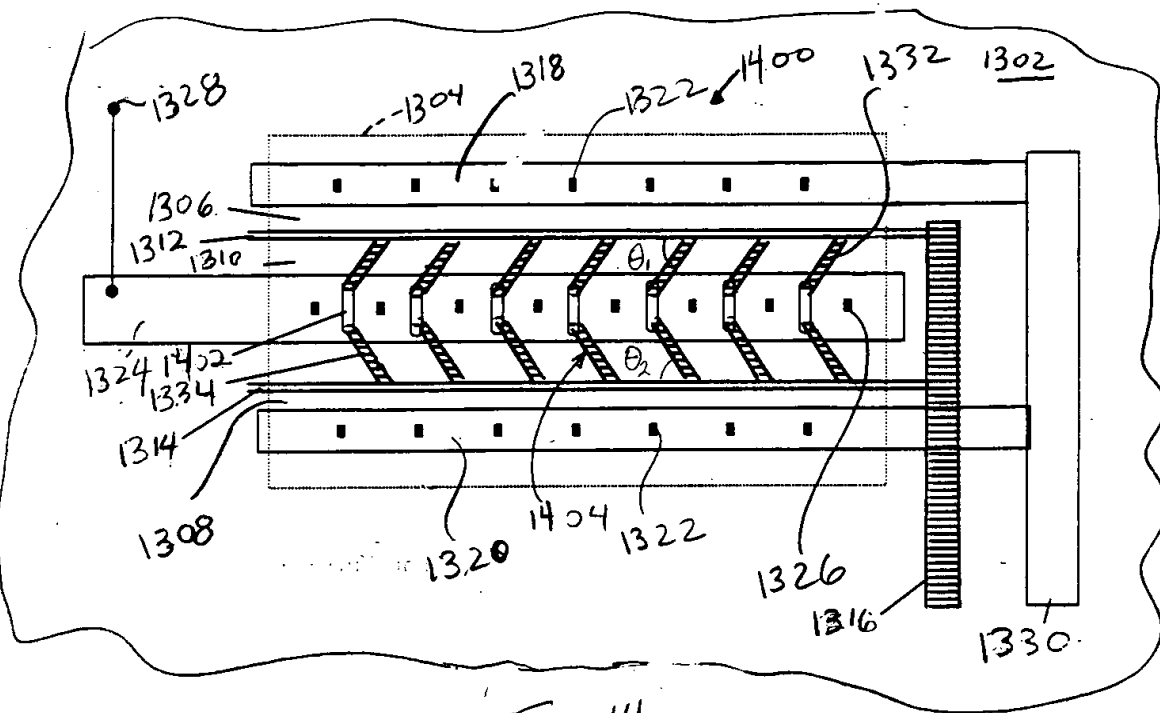


Fig. 14

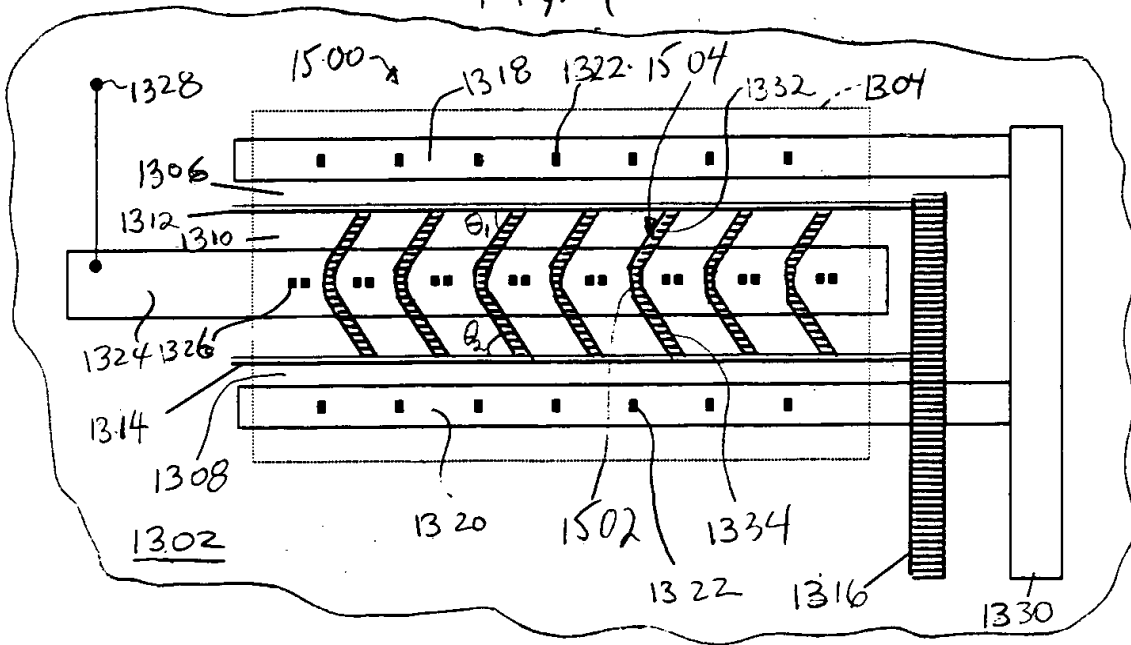
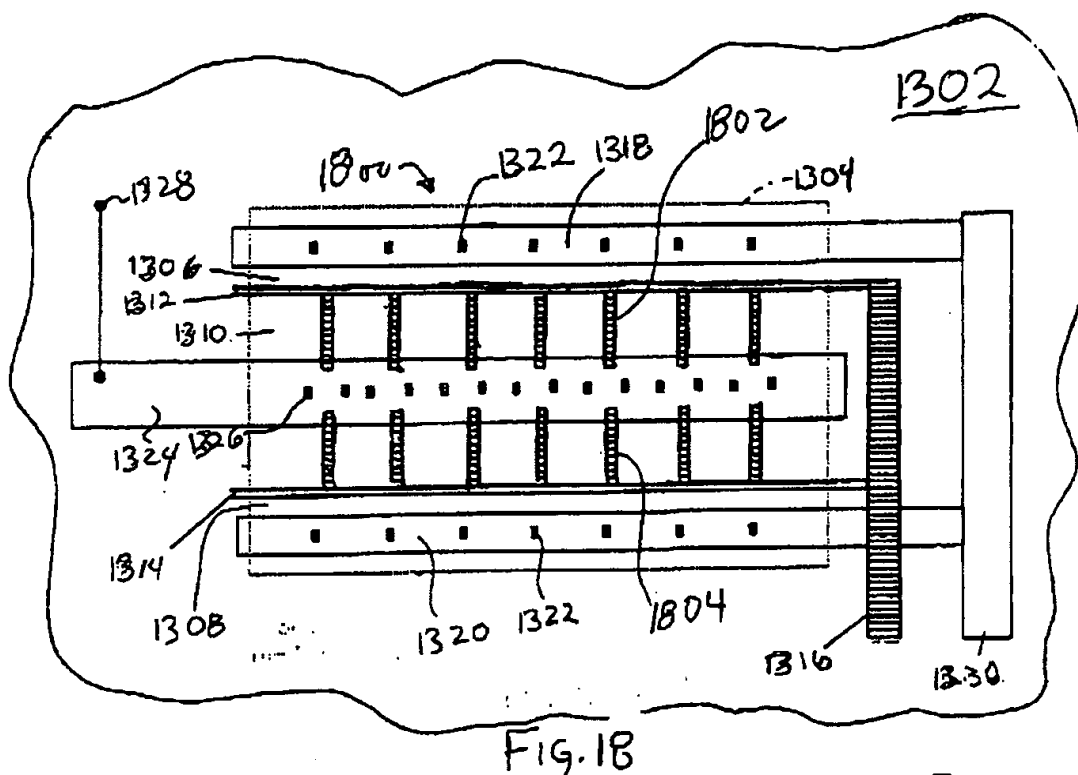
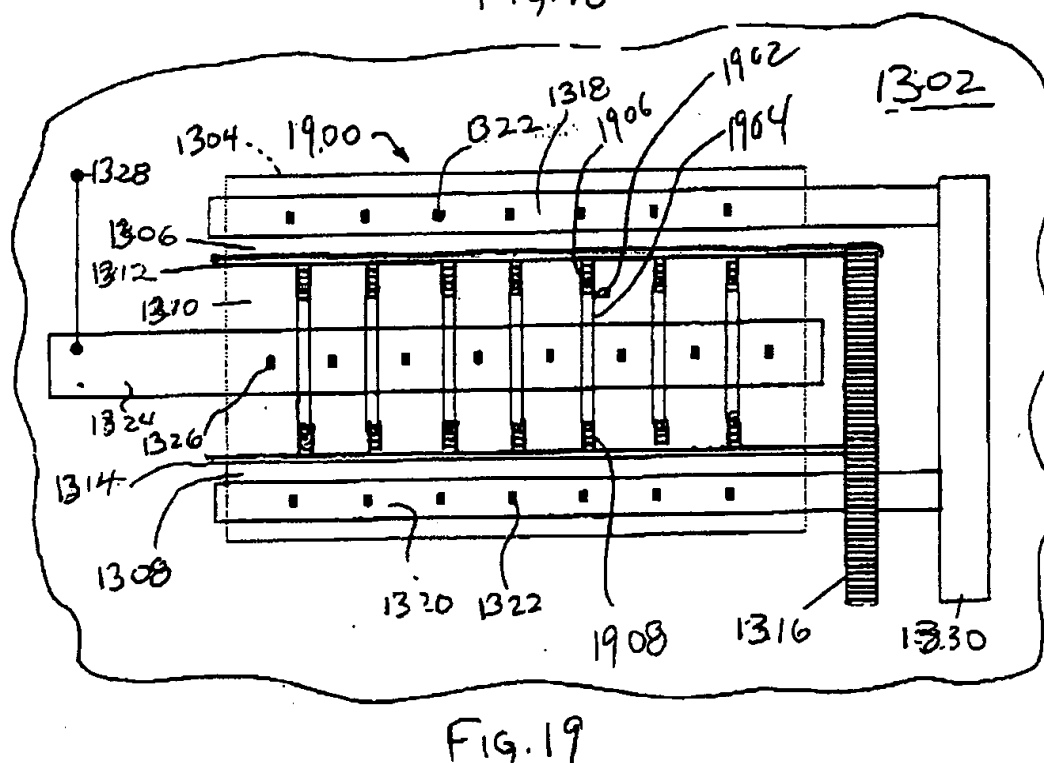


Fig. 15





S. of 12-14 2000  
CHL Dec. 14, 2000  
WFC Dec. 14, 2000  
WYL Dec. 16, 2000



N.L. 12-14, 2009  
CHL. Dec. 14, 2006  
WFC. Dec. 14, 2000  
WYL. Dec. 16, 2000

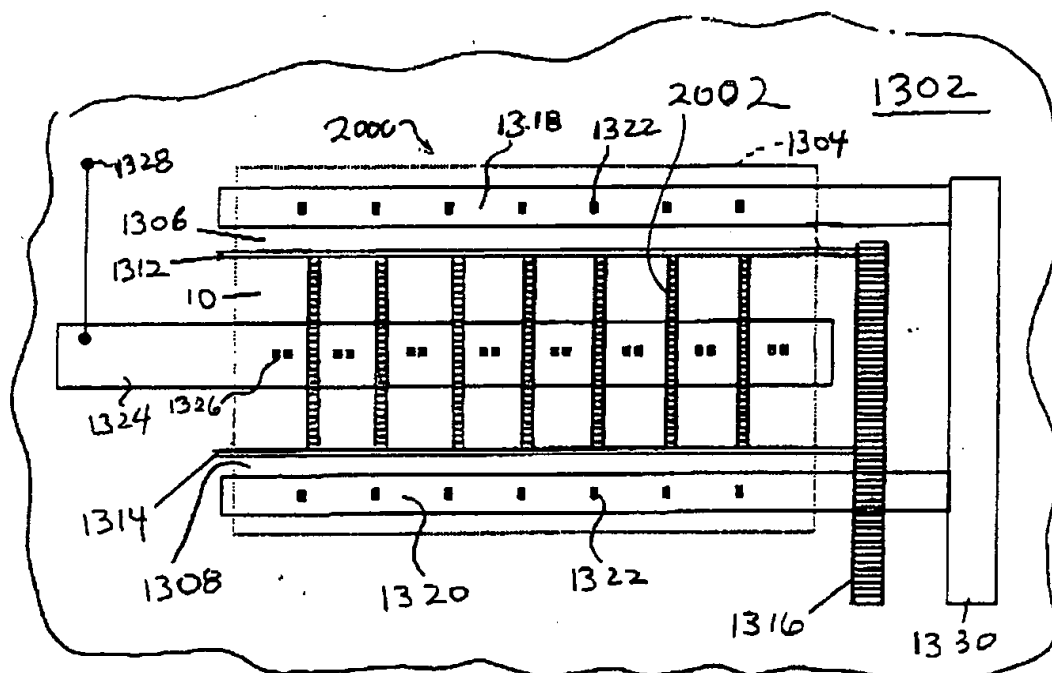


FIG. 20

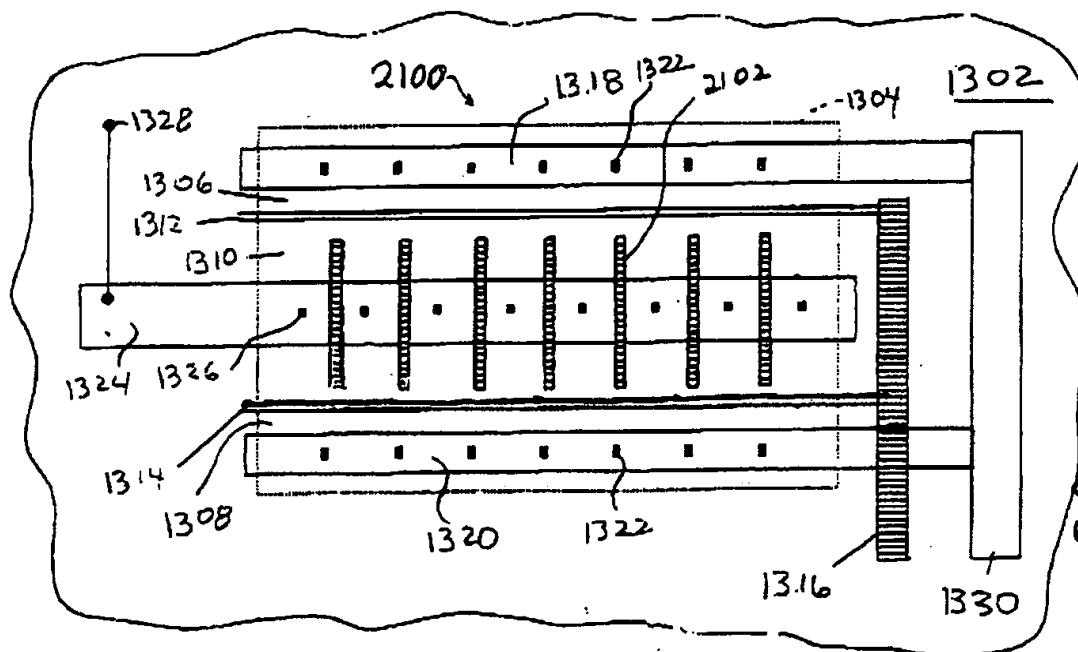


Fig. 21

S.L. 12-14, 2000  
C.H.L. Dec. 14, 2000  
L.F.C. Dec. 19, 2000  
W.Y.L. Dec. 16, 2000

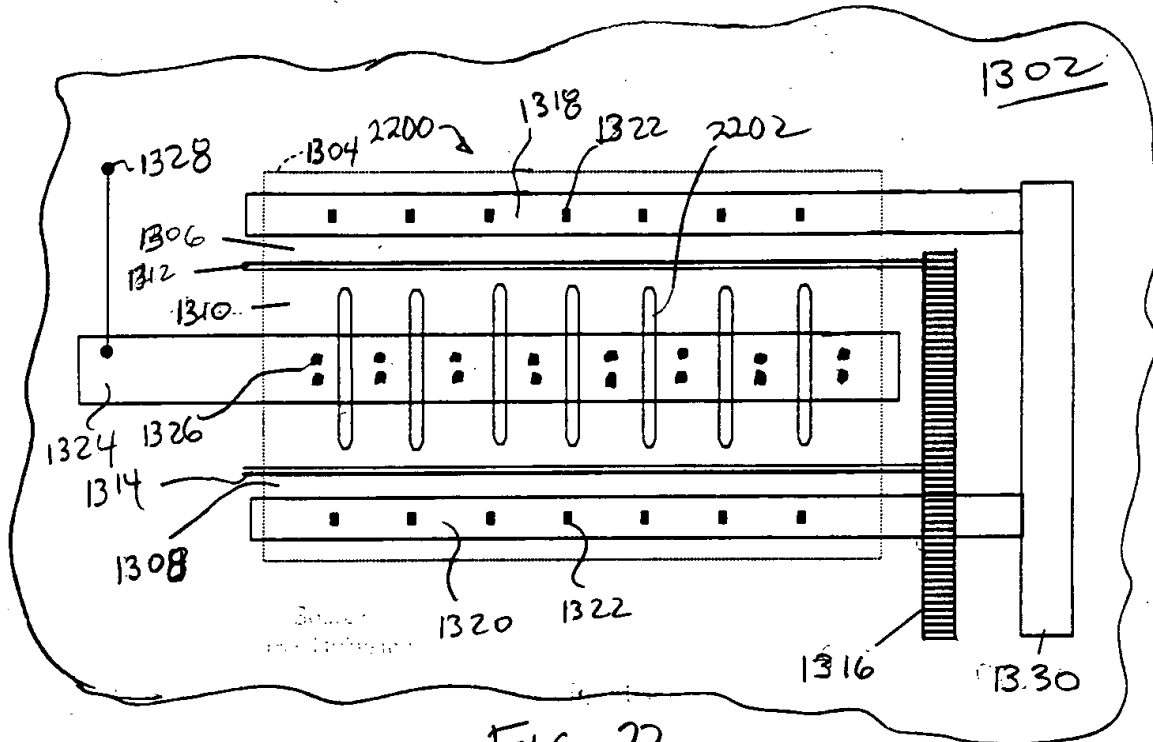


FIG. 22

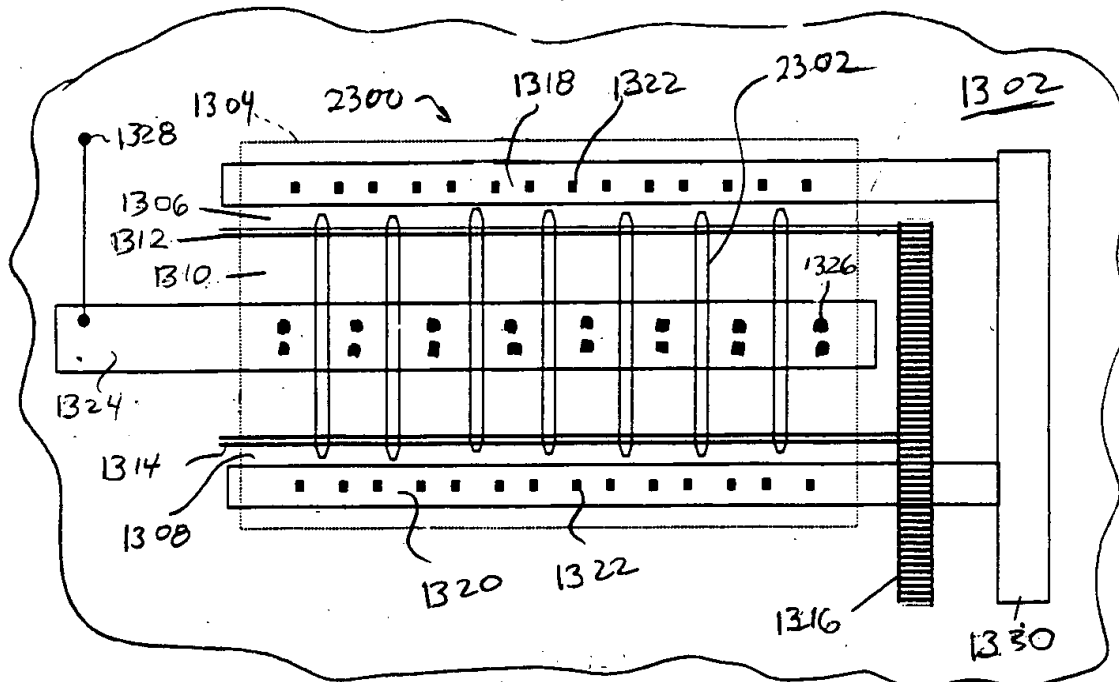


FIG. 23

SECRET 57034260

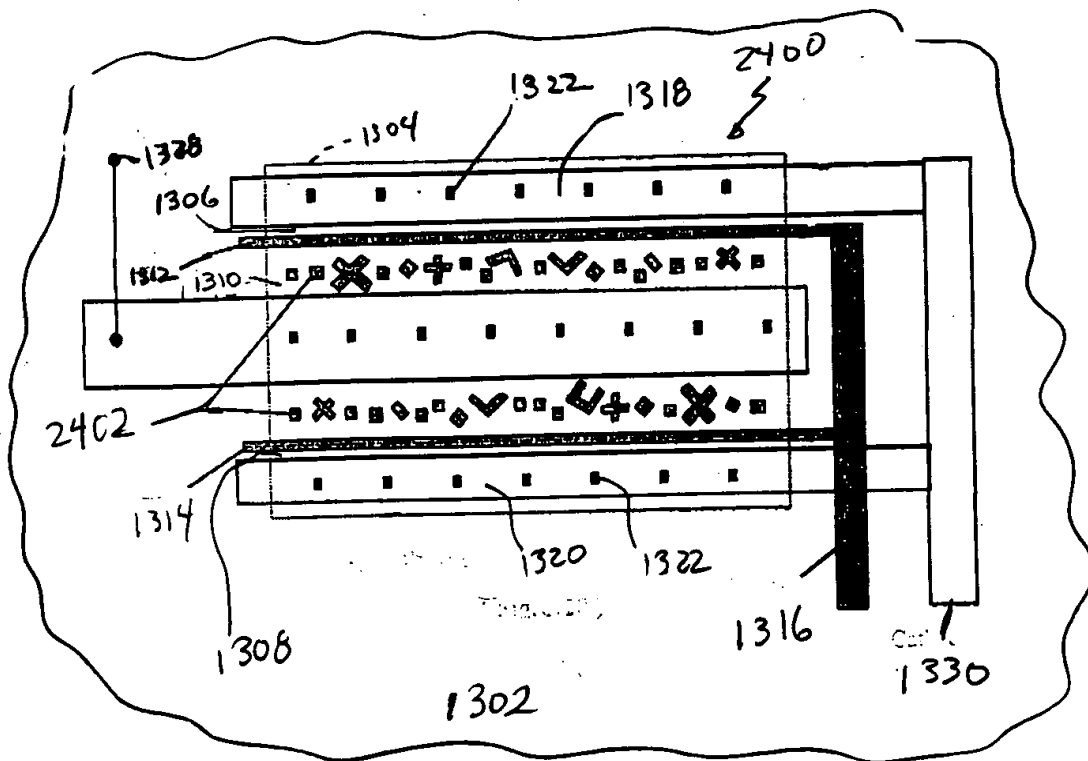


FIG. 24

SECRET 57064260

